

FIG. 1

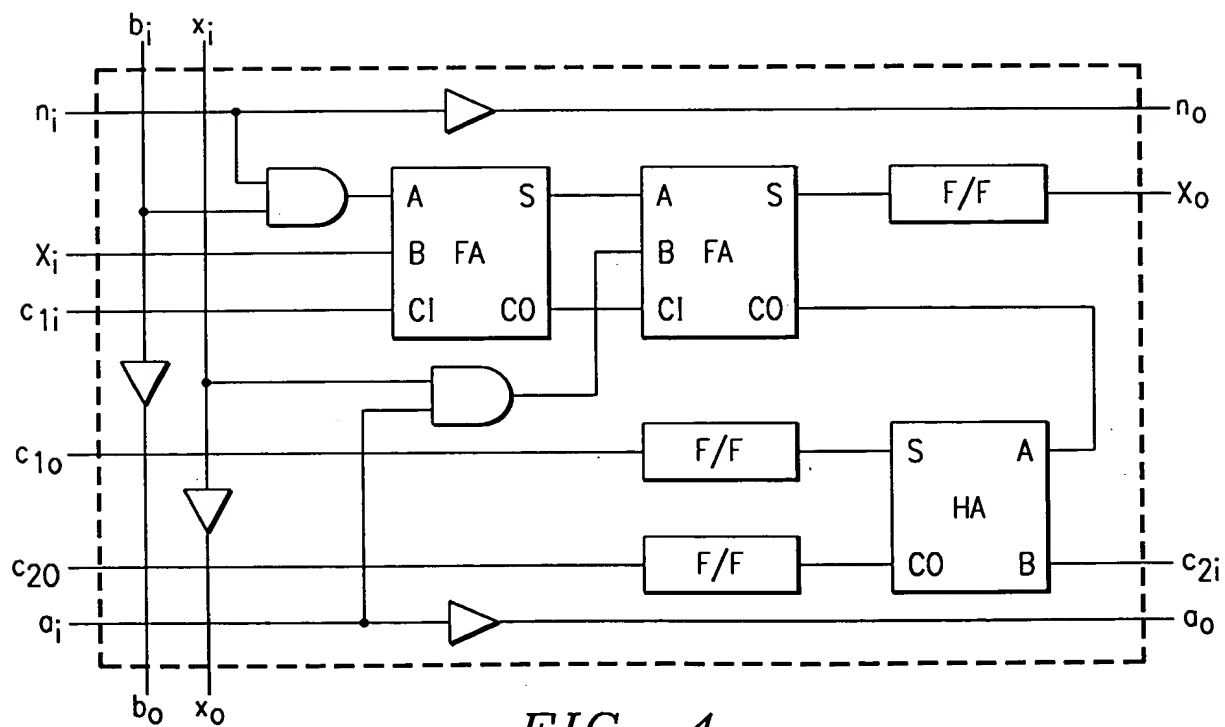


FIG. 4

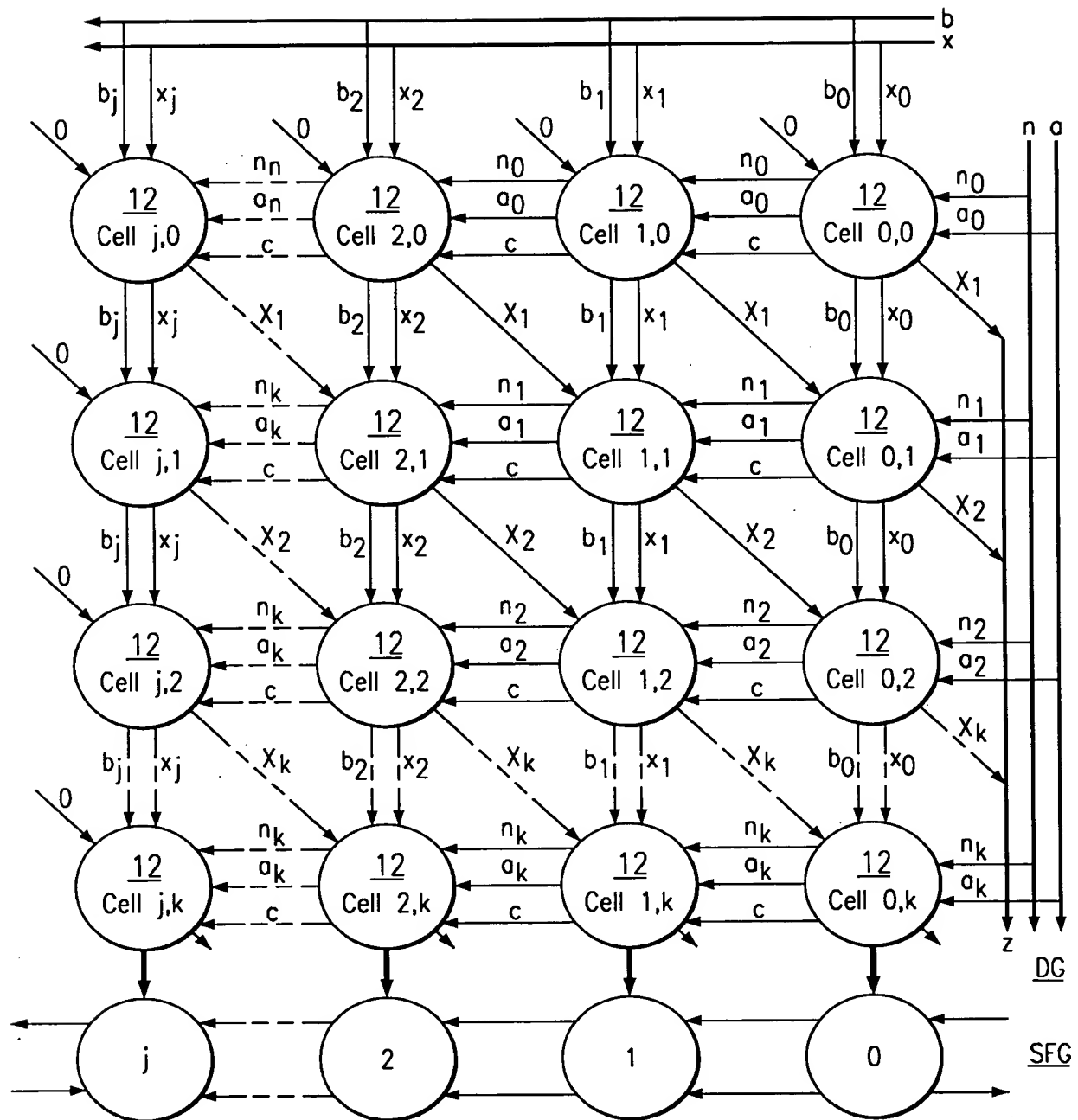


FIG. 2

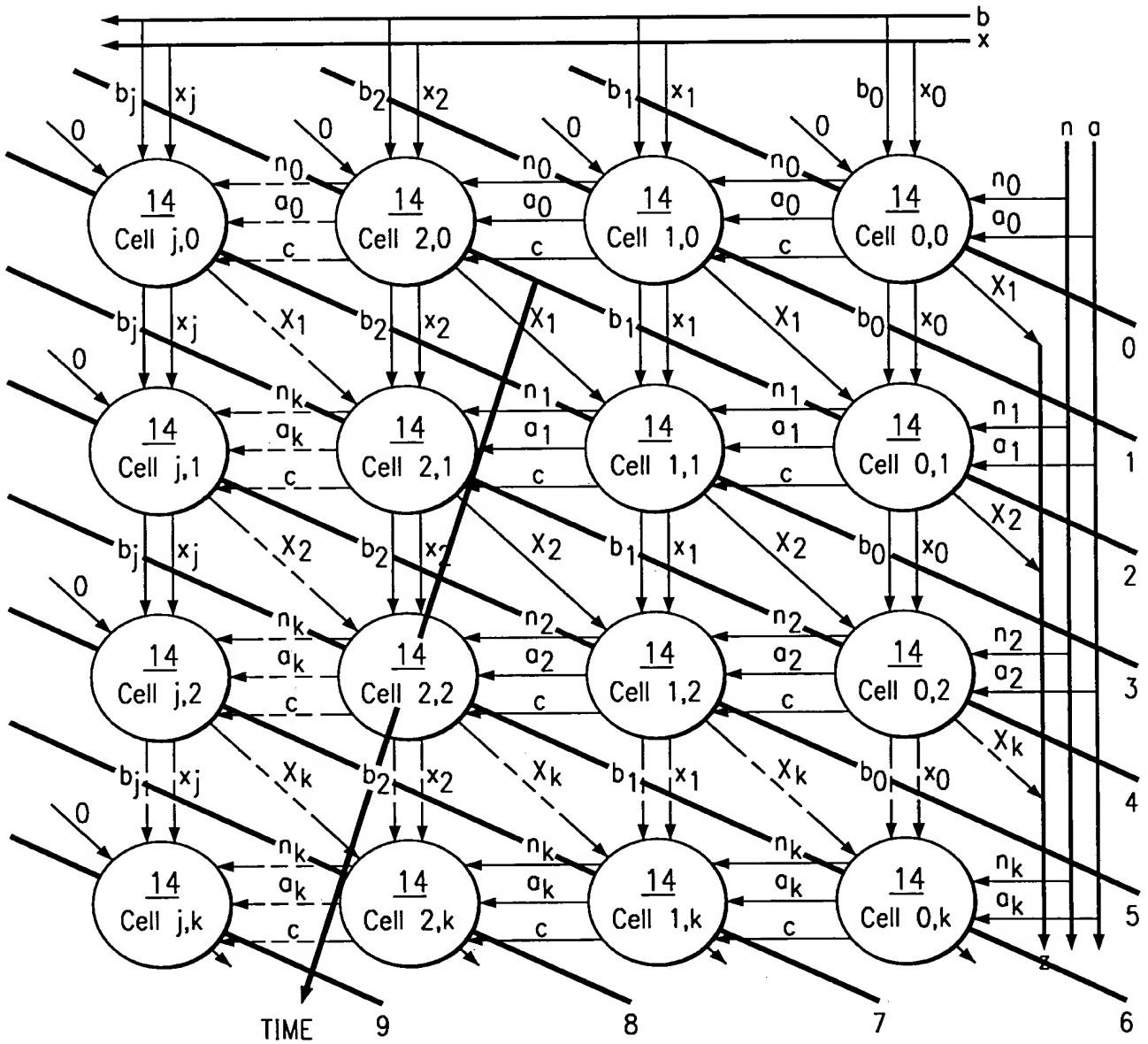


FIG. 3

00760-92089960

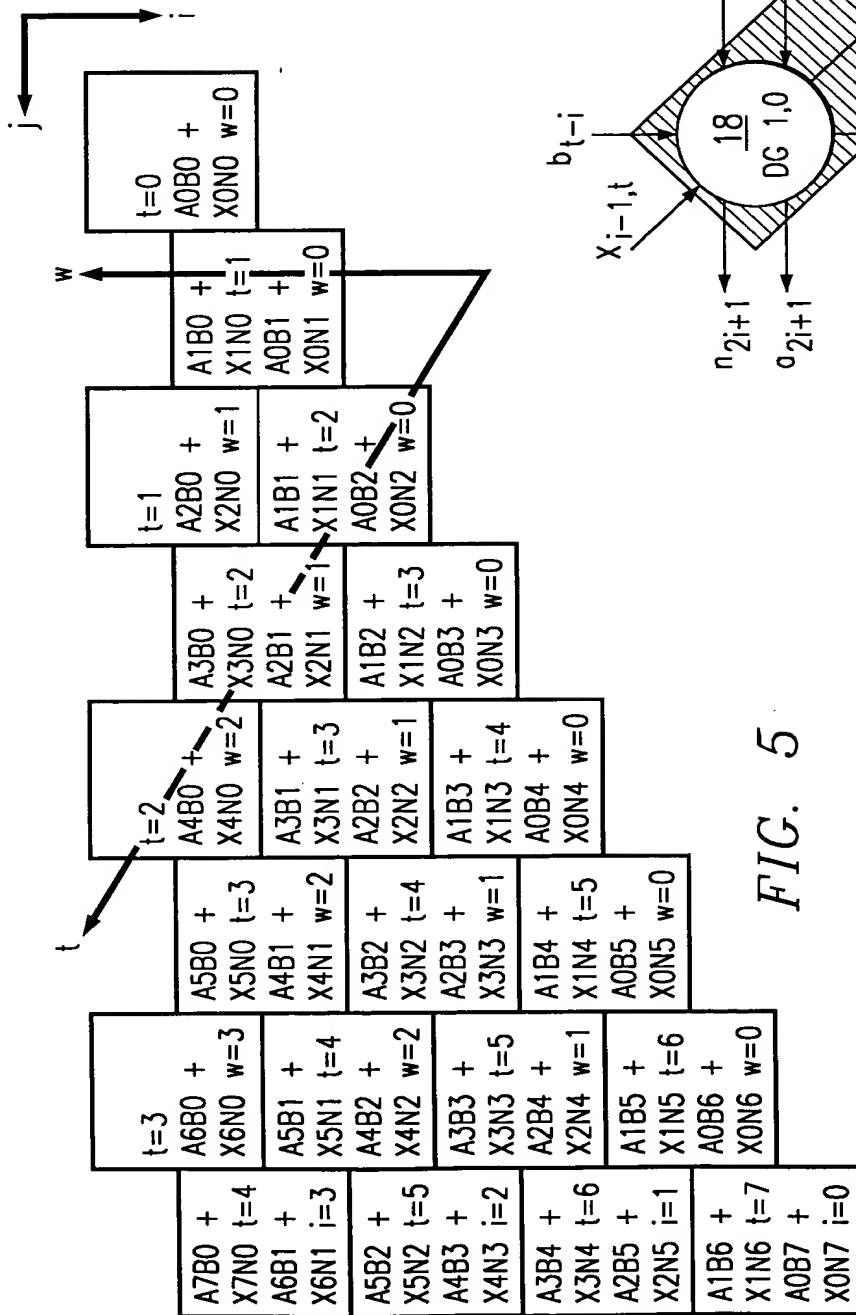


FIG. 5

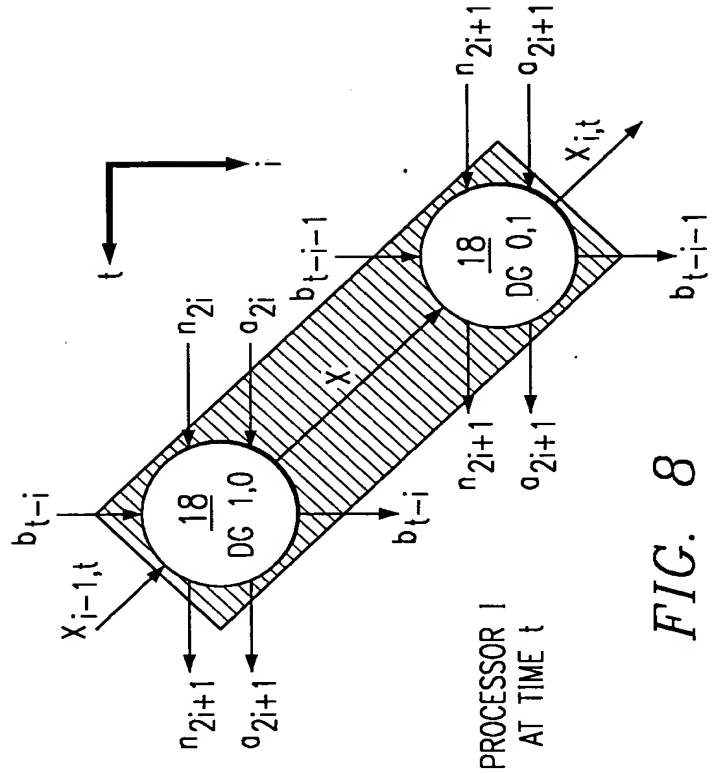


FIG. 8

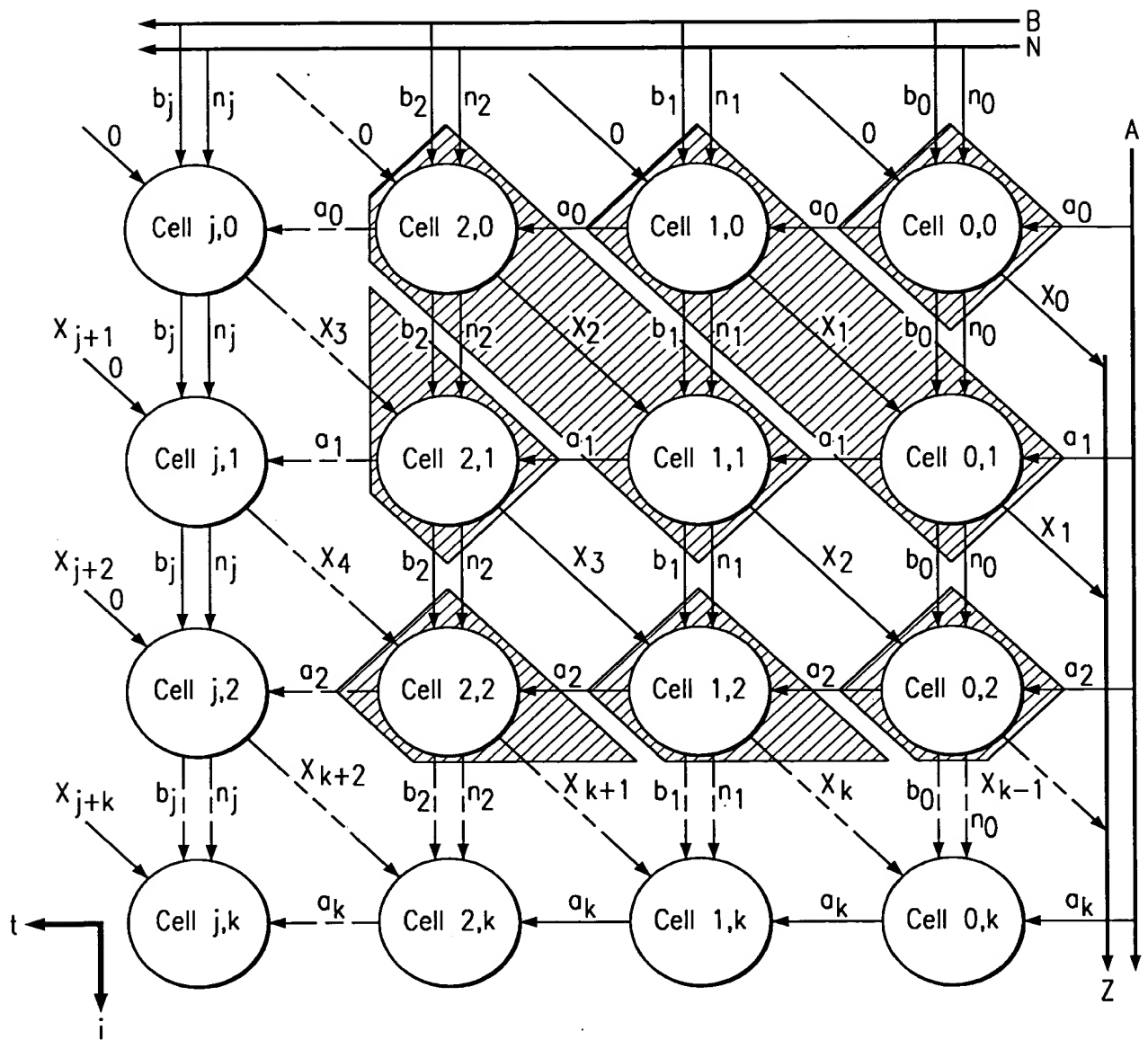


FIG. 6

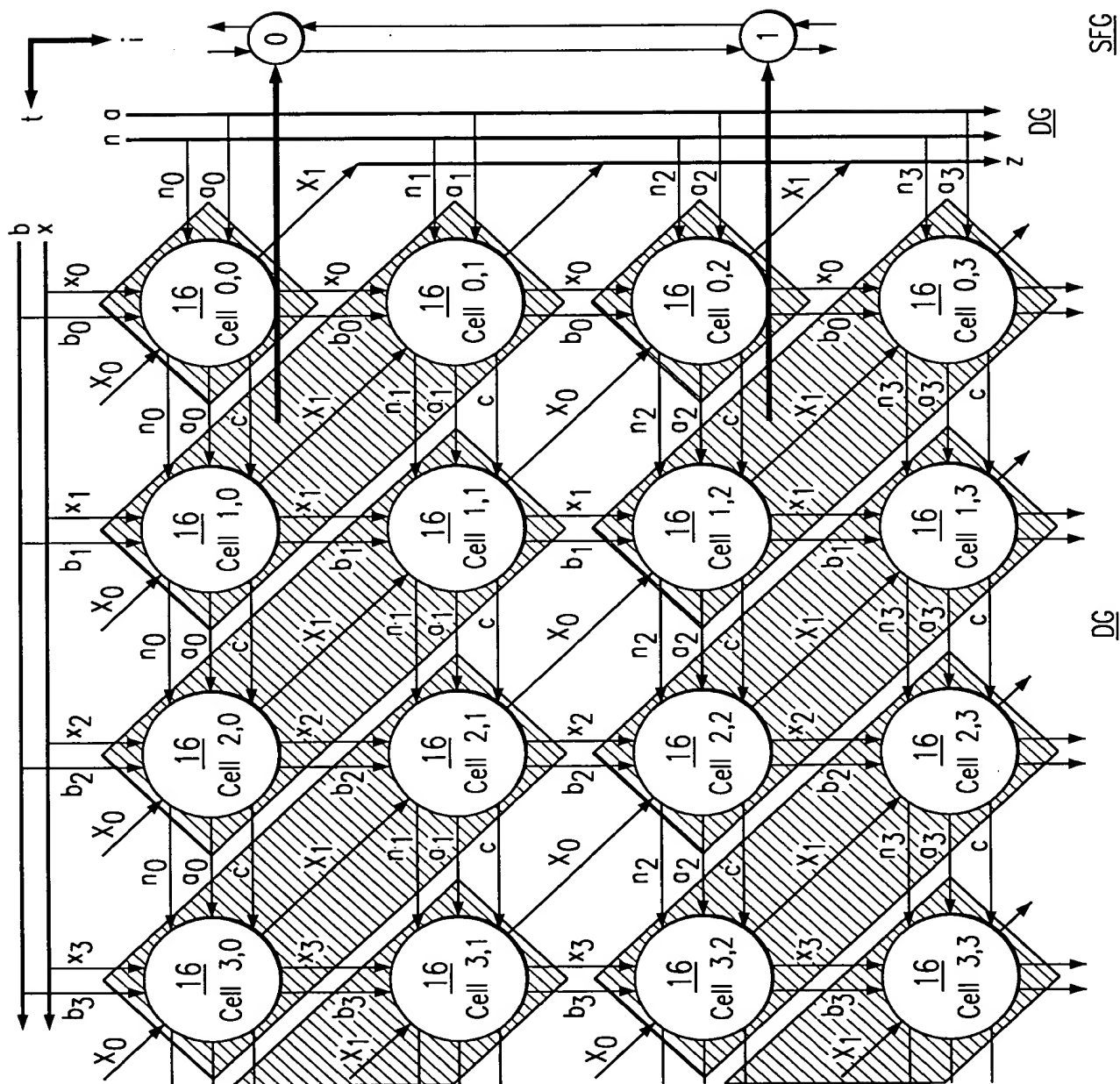
[illegible]

FIG. 7

SFG

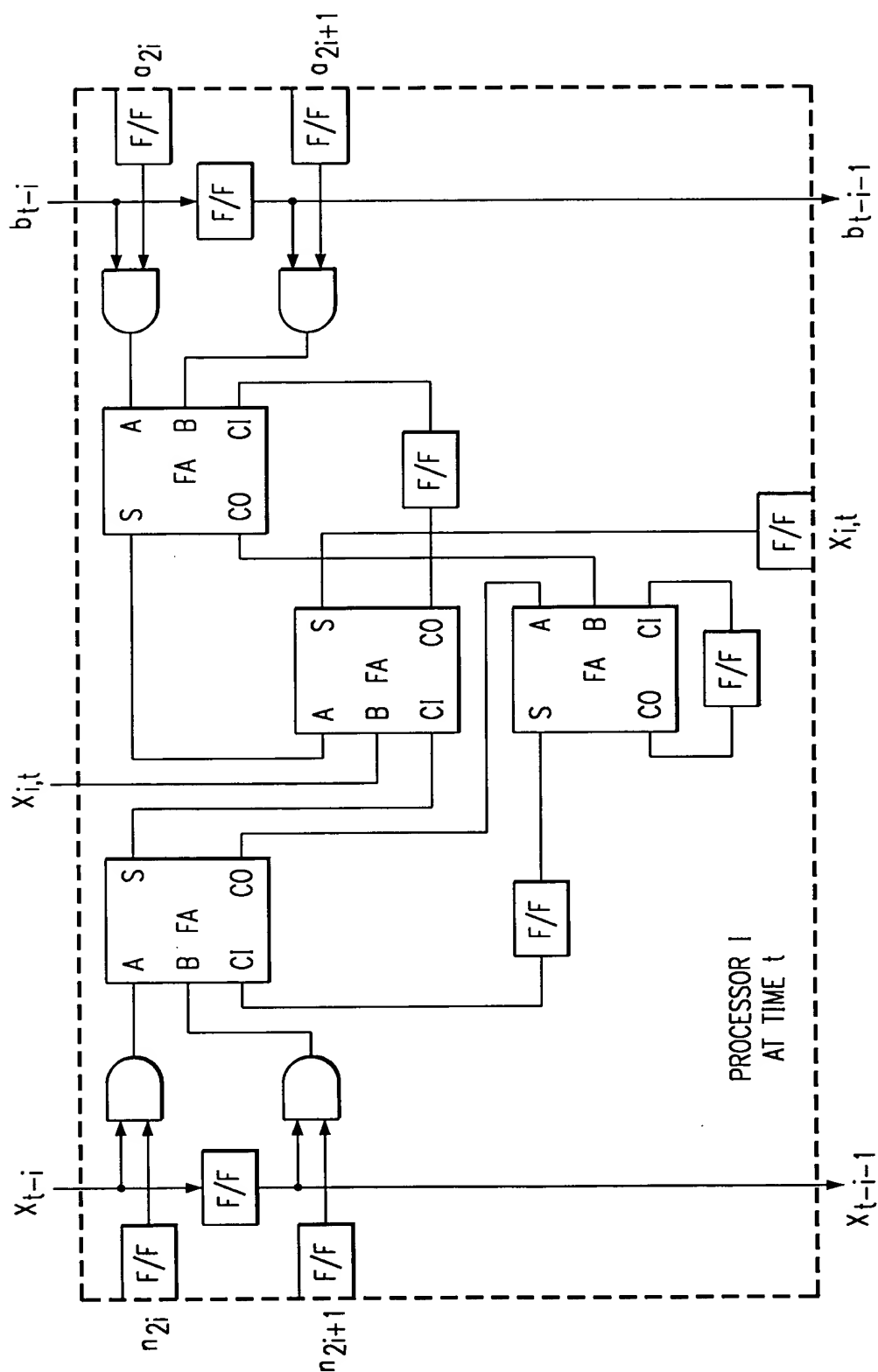


FIG. 9

Process TypicalBinaryMultiply (A,B)

Z:=0;

For i in 0 to n-1 loop

c := 0;

For j in 0 to n-1 loop

$Z_{i+j} := (Z_{i+j} + A_i * B_j + c) \bmod 2;$

$c := (Z_{i+j} + A_i * B_j + c) \div 2;$

end loop;

for j in n to 2n-1 loop

$Z_j := (Z_j + c) \bmod 2;$

$c := (Z_j + c) \div 2;$

end loop;

transmit  $Z_i$ ;

end loop;

Process Reduce( $Z_i$ , N)

c := 0;

For i in 0 to n-1 loop

wait for  $Z_i$ ;

$X_i := Z_i$ ;

$X_i := (X_i + x * N_i + c) \bmod 2;$

$c := (X_i + x * N_i + c) \div 2;$

end loop;

$X := X/2;$

For i in 1 to k-1 loop

$x = X \bmod 2;$  c := 0;

For j in 0 to n-1 loop

$X_j := (X_j + x * N_j + c) \bmod 2;$

$c := (X_j + x * N_j + c) \div 2;$

end loop;

$X = X/2;$

end loop;

BITS OF Z FEED  
SEQUENTIALLY  
ACROSS

FIG. 10

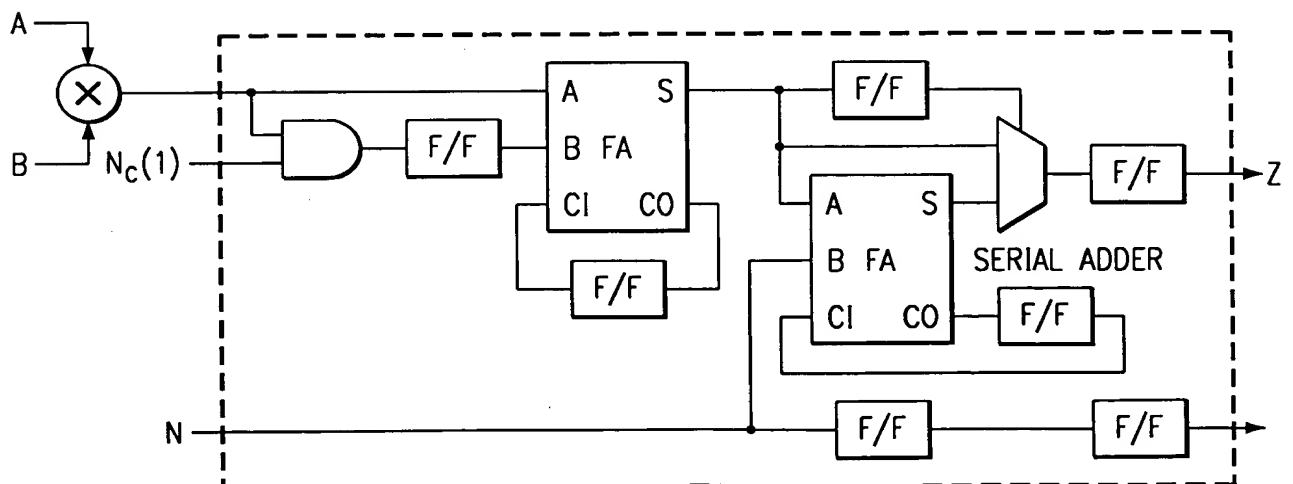
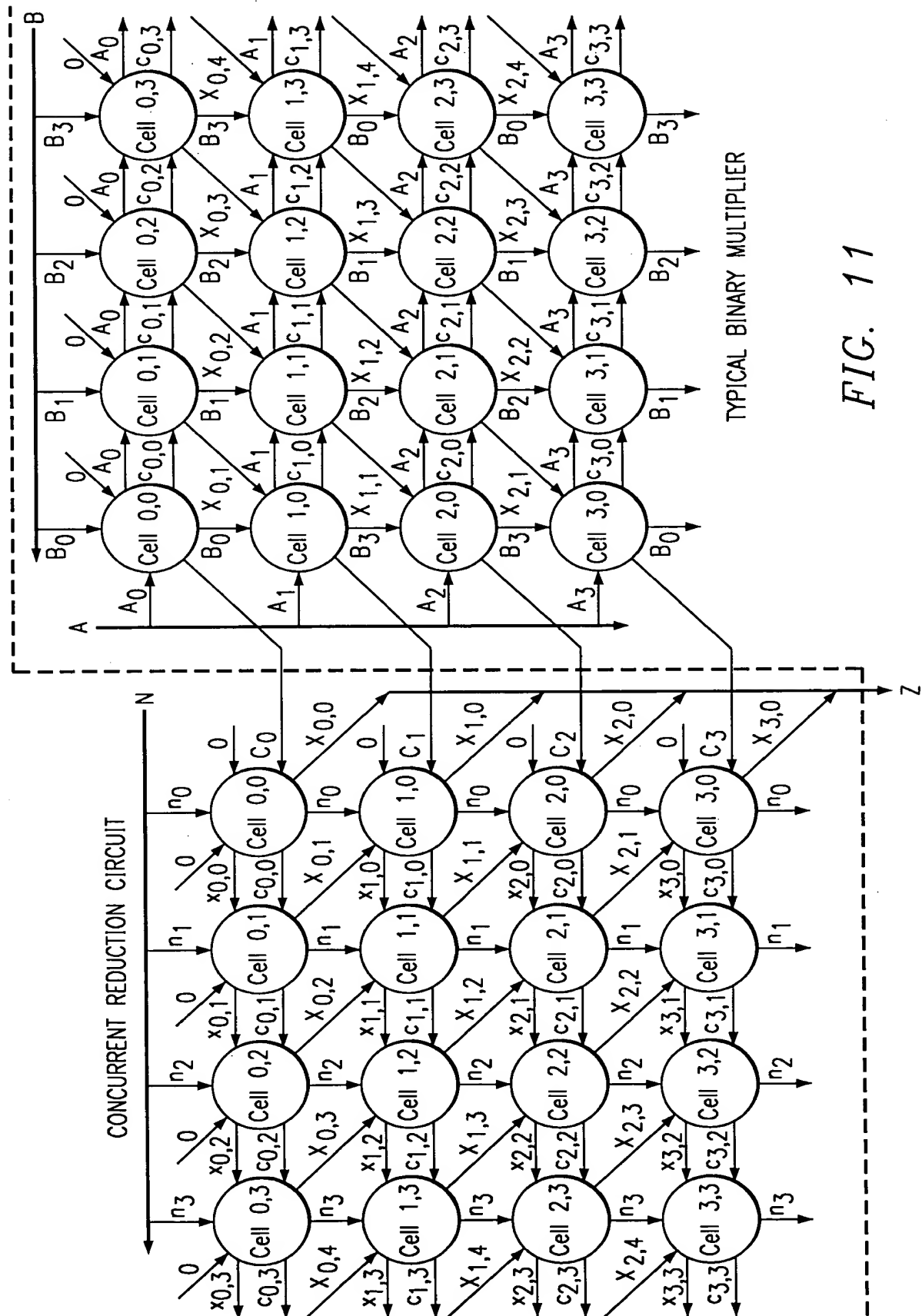


FIG. 18





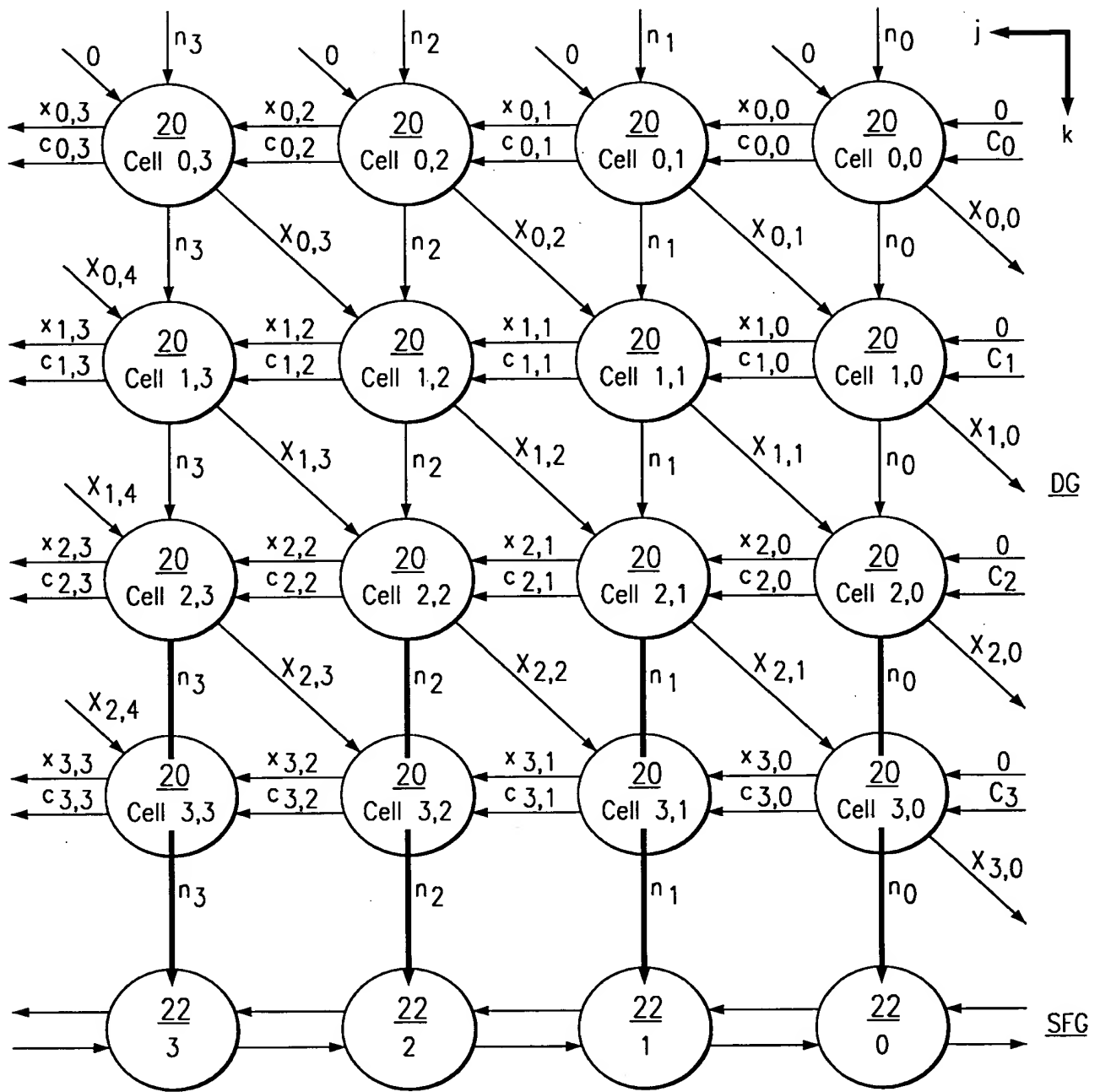


FIG. 12

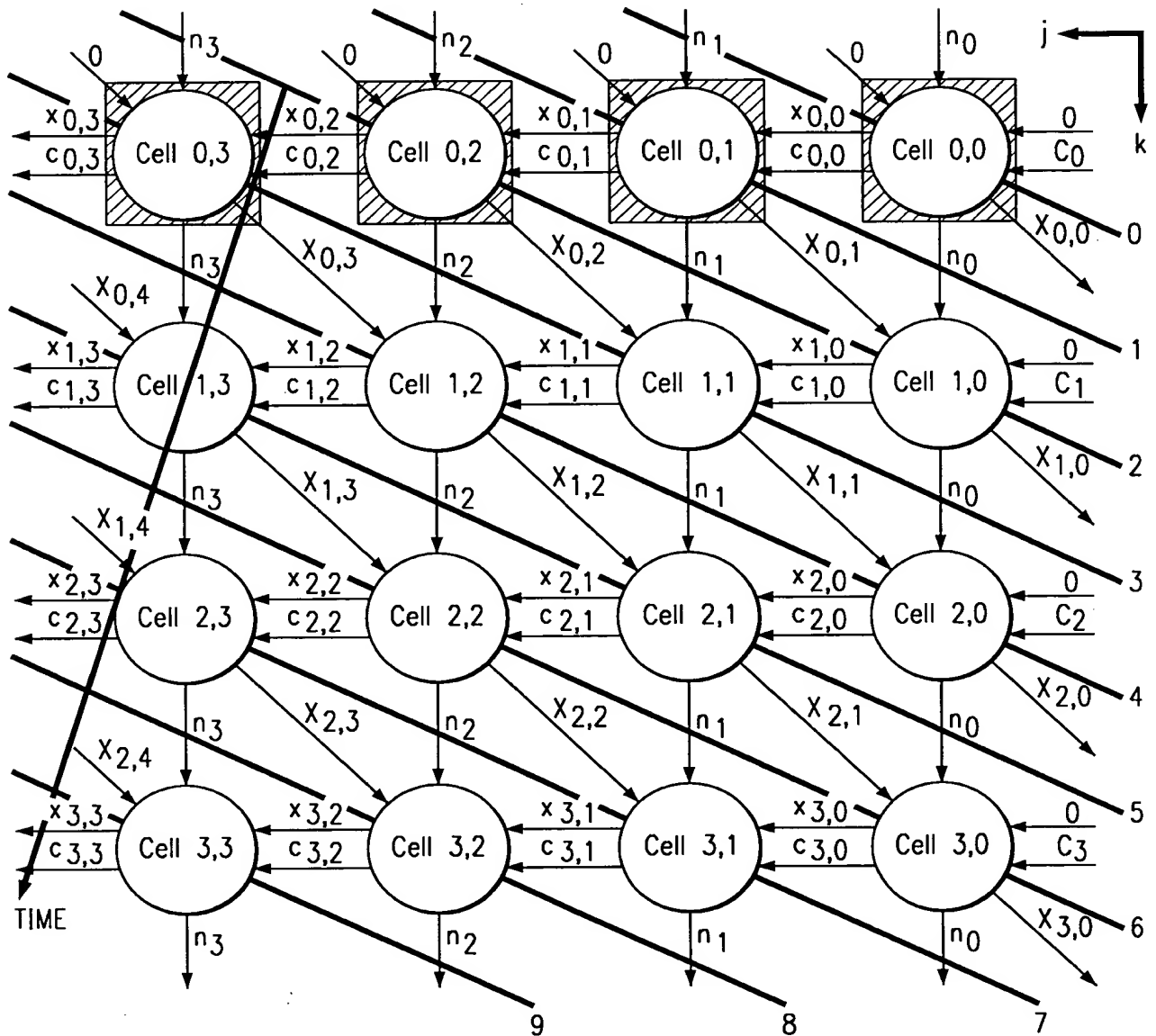


FIG. 13

FIG. 14

The diagram illustrates a parallel processing system with three stages, labeled  $n_1$ ,  $n_2$ , and  $n_3$ , and a final stage. Each stage is enclosed in a dashed box and contains the following components:

- Input and Delay:** An input signal  $x_0$  is fed into a delay block (24) and an AND gate (26). The output of the delay block is  $x_i$ .
- AND Gate:** The AND gate (26) takes  $x_i$  and a carry-in signal  $c_i$  as inputs. Its output is  $x_0$ .
- Multiplexer:** The multiplexer (28) has two inputs:  $x_0$  and  $x_i$ . It is controlled by a select signal  $S$ . Its output is  $x_0$ .
- Flip-Flop:** The flip-flop (30) takes  $x_0$  as input and produces the carry-out signal  $c_o$ .

The carry-out signal  $c_o$  from one stage is fed into the carry-in signal  $c_i$  of the next stage. The final stage also includes a delay block (24) and a flip-flop (30) to produce the final output  $x_0$ .

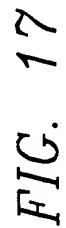
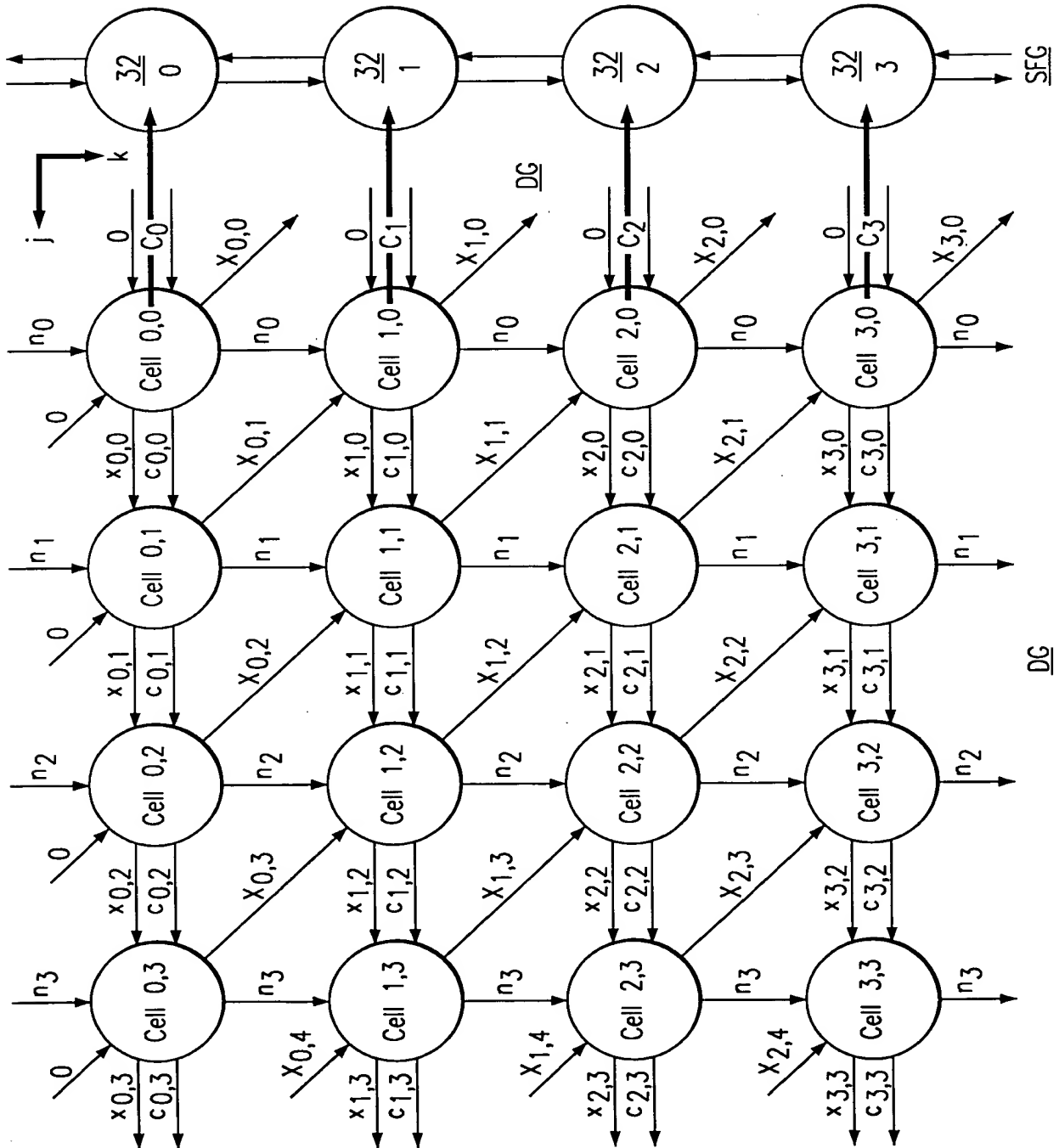


FIG. 15



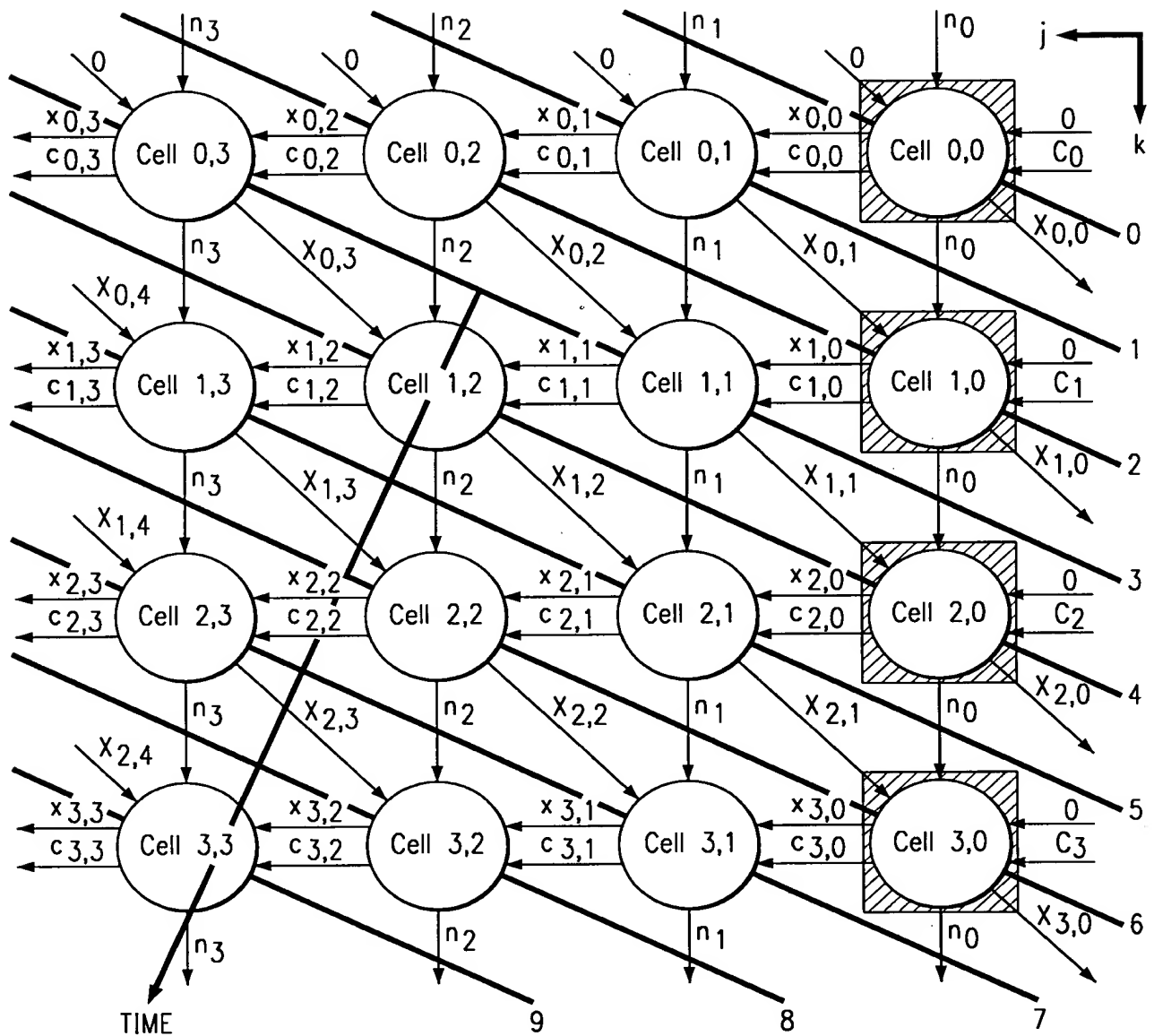
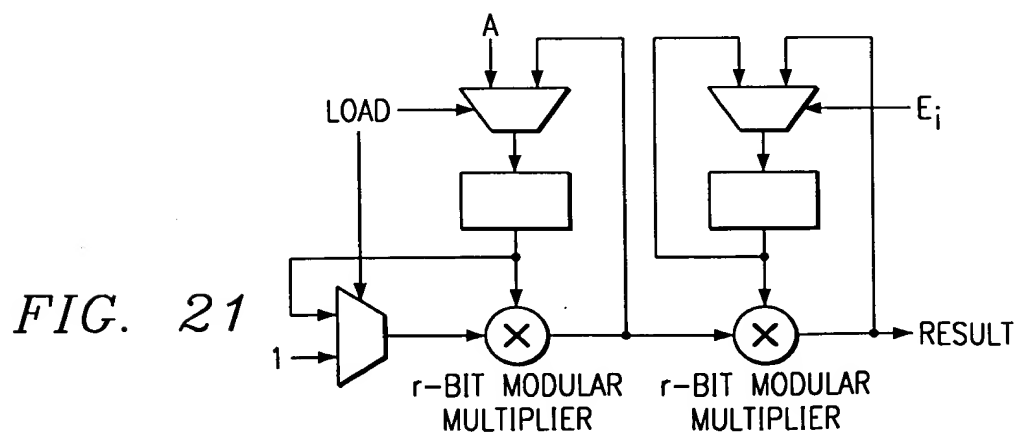
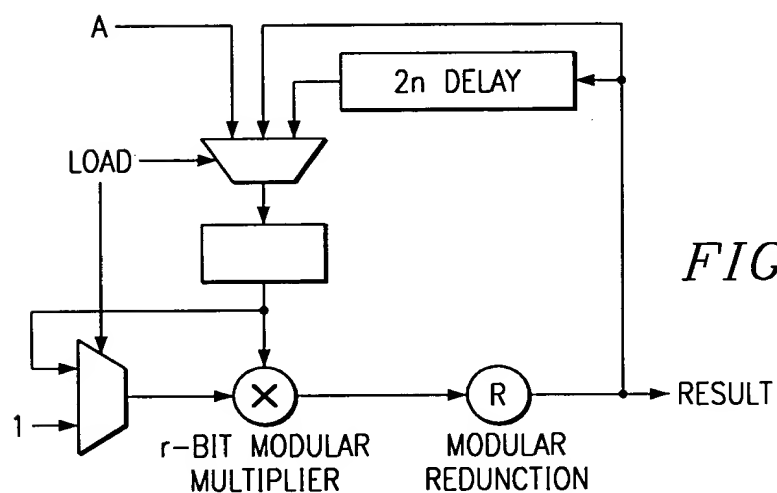
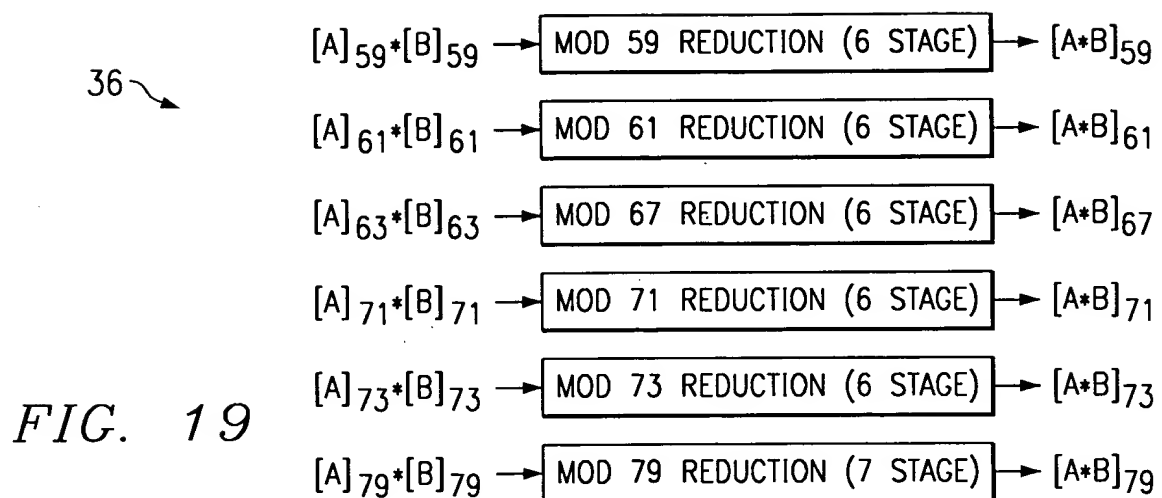


FIG. 16



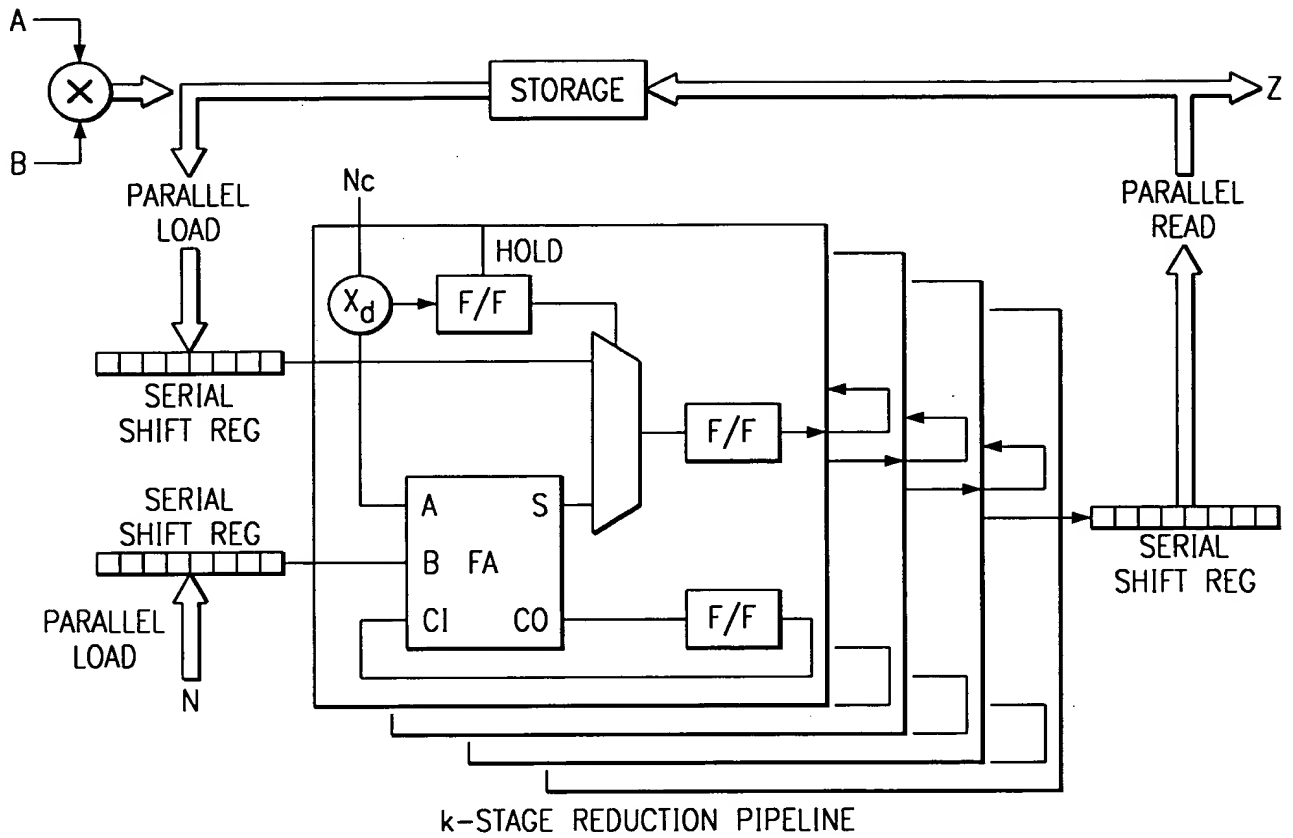


FIG. 22

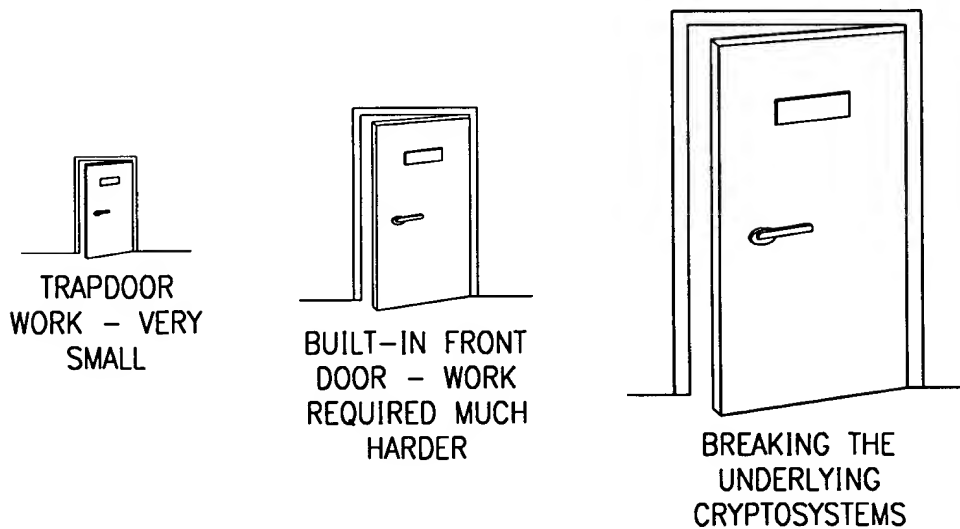


FIG. 23



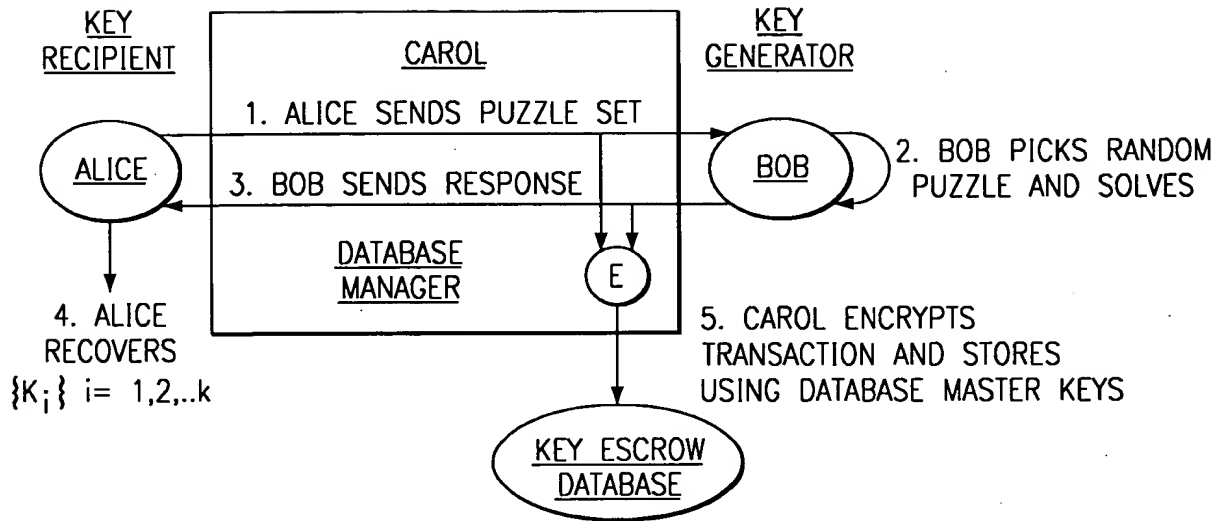


FIG. 24

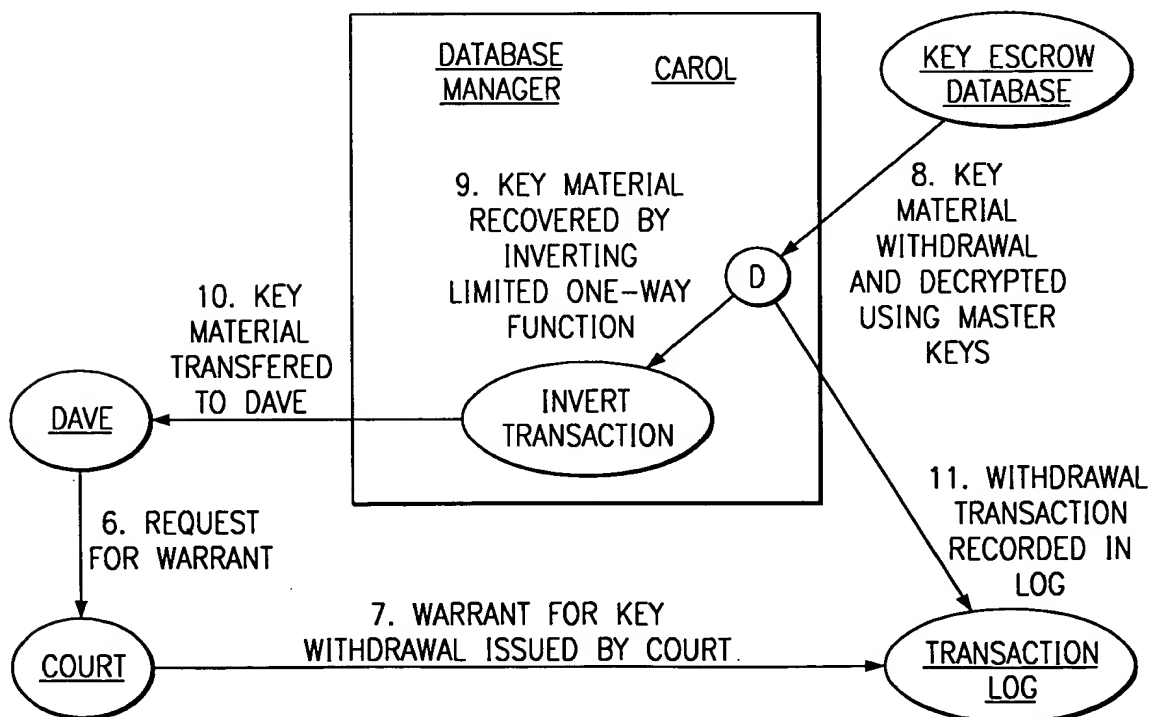


FIG. 25

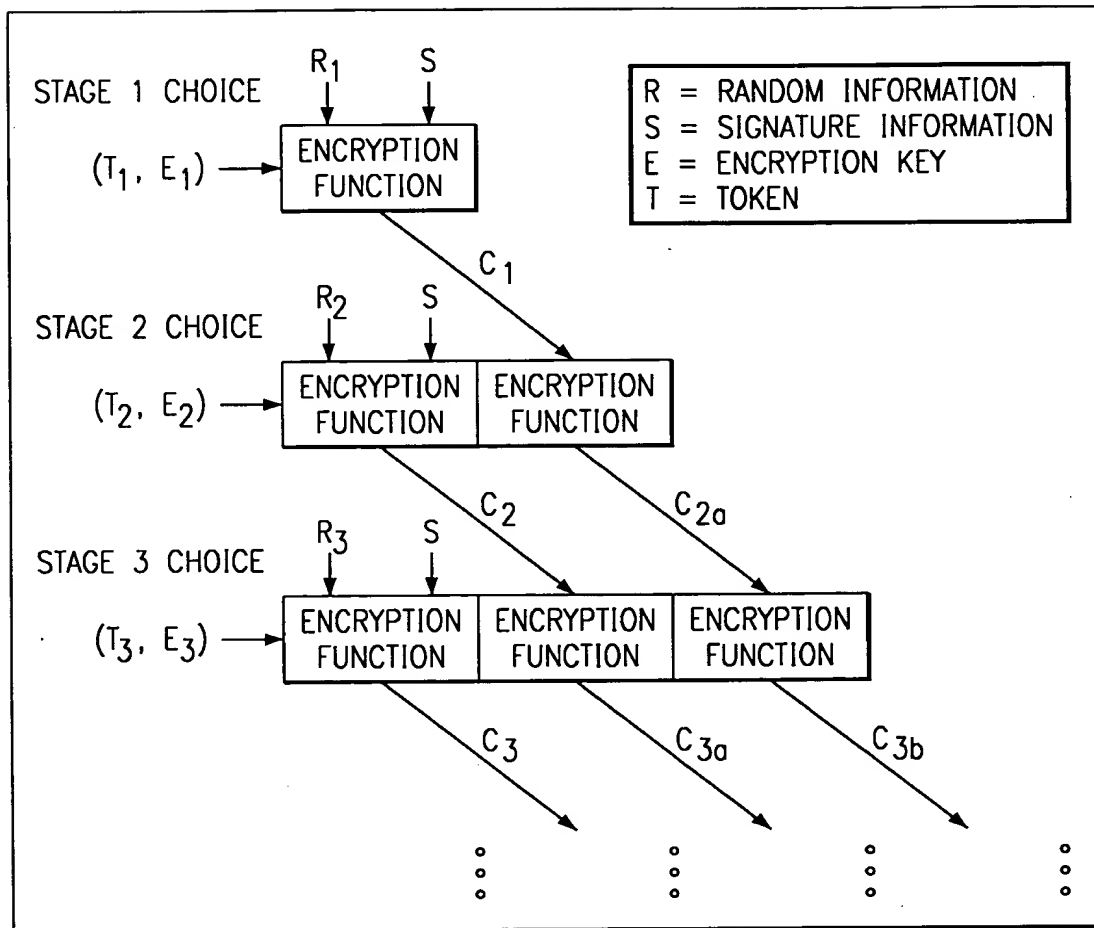


FIG. 26

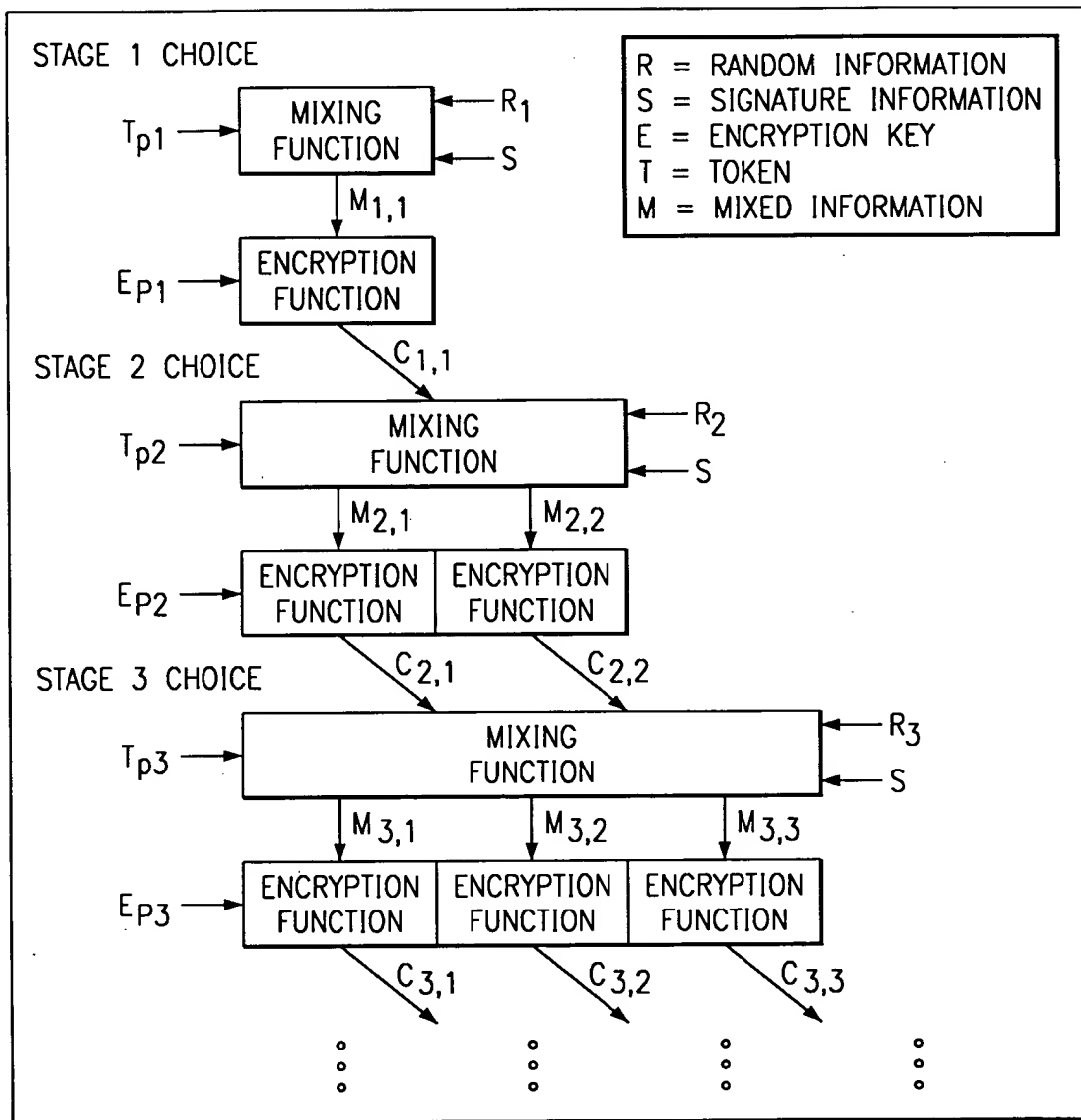


FIG. 27